connected in series with a host controller, to form a system shift register. The nodes are serially addressed by a serial data message from a DATA OUT line of the host controller, which message includes MxN data bits followed by a strobe indicator, where N is the number of nodes and M is the number of devices at each node. All controllers are connected to a V+ line and a COMMON line and a RETURN line. The system register forms a fourth line, with one end connected to the host controller DATA OUT terminal and the other end connectable to the RETURN line.

IN THE CLAIMS:

Please amend claims 11, 13, 15, 21, 22, 24, 31, 32 and 35, respectively, to read as follows:

11. (Amended) The gaming system of claim 8, wherein the devices include switches and LEDs, the output signal including data bits for causing the local controllers to record the states of the switches and data bits for causing the local controllers to control the states of the LEDs.

13. (Amended) A gaming system comprising:

a plurality of devices to be individually accessed, arranged in a string of N nodes, with each node including up to M of the devices, wherein M and N are whole numbers greater than one;

a host controller having a data out terminal;

a plurality of local controllers respectively associated with the nodes,

each local controller having a data in terminal and a data out terminal and including a M-bit shift register with the register positions respectively connected to device output terminals to which the devices of the associated node may respectively be connected;

the data out terminal of the host controller being connected to the data in terminal of a first node and the data in terminal of each of the other nodes being connected to the data out terminal of the preceding node in the string so that the string of nodes provides a (MxN)-bit shift register;

the host controller producing at its data out terminal an output signal comprising a serial digital data stream including MxN bits followed by a strobe indicator so that the MxN bits are sequentially loaded into and fill the (MxN)-bit register;

each local controller being responsive to the strobe indicator for utilizing the contents of its M-bit register for accessing the associated devices.

15. (Amended) The gaming system of claim 14, wherein M is 4.

21. (Amended) The gaming system of claim 13, wherein the output signal is comprised of bytes each having at least one M-bit segment.

22. (Amended) The gaming system of claim 21, wherein consecutive M-bit segments of a byte respectively address consecutive nodes.

24. (Amended) A gaming system comprising:

a plurality of devices to be individually accessed including one or more first devices to be sensed and one or more second devices to be controlled, the devices being arranged in a string of N nodes with each node including up to M of the devices, wherein M and N are whole numbers greater than one;

a host controller having a data out terminal and a data in terminal;

a plurality of local controllers respectively associated with the nodes,

each local controller having a data in terminal and a data out terminal and including a M-bit shift register with the register positions respectively connected to device output terminals to which the devices of the associated node may respectively be connected;

the data out terminal of the host controller being connected to the data in terminal of a first node and the data in terminal of each of the other nodes being connected to the data out terminal of the preceding node in the string so that the string of nodes provides a (MxN)-bit shift register, and the data out terminal of a last node being connected to the data in terminal of the host controller;

the host controller producing at its data out terminal an output signal comprising a serial digital data stream including MxN bits followed by a strobe indicator so that the MxN bits are sequentially loaded into and fill the (MxN)-bit register,

each local controller being responsive to the strobe indicator for: (a) for each of its register positions connected to a first device, loading into that register position a bit indicative of the current state of the first device; and (b) for each of its register positions connected to a second device, latching the contents of that position to its associated device output terminal for controlling the associated second device.

31. (Amended) A method for individually accessing each of a plurality of devices in a gaming system comprising:

grouping the devices into N nodes, with each node including a local controller and up to M devices connected to the local controller, wherein M and N are whole numbers greater than one,

connecting the local controllers in series with one another and with a data out terminal of a host controller so that the local controllers cooperate to define an (MxN)-bit shift register,

providing a power line connected to all of the controllers and a common line connected to all of the controllers, and

transmitting from the host controller data out terminal to all of the local controllers a serial digital data message including MxN bits respectively corresponding to the devices for individually controlling the devices.

32. (Amended) The method of claim 31, wherein the data message terminates with a strobe indicator which causes each local controller to access the devices connected thereto in accordance with bits of the data message corresponding to that local controller.

35. (Amended) The method of claim 34, wherein each digital data message terminates with a strobe indicator, and each local controller responds to the strobe indicator for storing, for each at least one device connected thereto, a data bit corresponding to the current state of the at least one device, the stored bits being shifted from the register in response to a next data message from the host controller.

REMARKS

Attached hereto is a sheet entitled "Version of Abstract to Show Changes Made", setting forth the amended Abstract with editorial markings.

Attached hereto are sheets entitled "Version of Claims Marked to Show Changes Made", setting forth the amended claims with editorial markings.

Reconsideration of the rejected claims is respectfully asked.

The Abstract has been amended to be limited to 150 words in accordance with the examiner's requirement.

Claims 21 and 22 are rejected under 35 U.S.C. §112 as being indefinite in the use of the phrase "$(N)2^x$ bits". Claim 21 has been amended to delete that language and to recite the output signal is comprised of bytes each having "at least one M-bit segment."